REMARKS

In the last Office Action, claims 1-5 were rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,274,905 to Mo in view of applicant's admitted prior art. The Examiner stated that in Fig. 6A Mo discloses a vertical MOS transistor comprising a semiconductor substrate 600 having a first conductivity type, a body region 604 having a second conductivity type formed on the substrate, a trench 602 formed through the body region, a gate insulating film 612 formed along a surface of the body region and a wall surface and bottom surface of the trench, a polycrystalline silicon gate 614 formed in the trench so as to be in contact with the gate insulating film and surrounded by the gate insulating film, a metal silicide gate 626 formed in the trench so as to be in contact with the polycrystalline silicon gate and surrounded by the gate insulating film and the polycrystalline silicon gate, a source region 608 having the first conductivity type formed on a surface of the body region and around the trench so as to be in contact with the gate insulating film, a gate electrode connected to the polycrystalline silicon and metal silicide gates, and a source electrode connected to the source region.

The Examiner acknowledged that Mo does not disclose an epitaxial growth layer of the first conductivity type

formed on the semiconductor substrate and a drain electrode connected to the semiconductor substrate, but pointed out that the admitted prior art shown in Fig. 2 discloses an epitaxial growth layer 2 of the first conductivity type formed on a semiconductor substrate and a drain electrode connected to the substrate. In view of this disclosure, the Examiner has taken the position that it would have been obvious to combine the teachings of the admitted prior art with Mo because forming a lightly doped layer of the first conductivity type has the known purpose of reducing the electric field between the source and drain regions.

By the present response, the specification has been revised in suitable respects to correct minor informalities and improve the wording. Elected claims 2-5 have been canceled without prejudice or admission and non-elected claims 6-9 have been canceled without prejudice to applicant's right to pursue the subject matter thereof in a continuing application. To obtain a fuller and more comprehensive scope of coverage, new claims 10-20 have been added.

Applicant respectfully submits that claims 1 and 10-20 patentably distinguish over the prior art of record.

The present invention relates to an improved vertical MOS transistor structure. As set forth by amended independent claim 1 and newly added independent claim 10, the

inventive vertical MOS transistor has a first conductivity type semiconductor substrate, a first conductivity type epitaxial layer formed on the substrate, a second conductivity type body region formed on the epitaxial layer, a trench formed through the body region to extend into the epitaxial layer, a gate insulator formed in the gate, and a gate formed in the trench. The gate is comprised of a first gate material partially filling the trench and a second gate material formed in a remaining portion of the trench not filled by the first gate material. In accordance with one aspect of the invention, the first gate material is polysilicon and the second gate material is one of silicon oxide and silicon nitride. In addition the inventive vertical MOS transistor has a first conductivity type source region formed in an upper surface of the body region surrounding the trench, a gate electrode connected to the gate, a source electrode connected to the source region and drain electrode connected to the semiconductor substrate.

Accordingly, the inventive vertical MOS transistor recited by independent claims 1 and 10 has a trench formed through a second conductivity body region and an epitaxial layer having the first conductivity type formed directly on a first conductivity type substrate. The gate fills the trench and is formed of first and second gate materials which

comprise polycrystalline silicon (claim 1) and an insulating material (claim 10) such as one of silicon oxide and silicon nitride (claim 1).

The claimed invention is disclosed in the embodiment shown in Fig. 11 of the application drawings. As shown, the vertical MOS transistor includes a first conductivity type semiconductor substrate 1, a first conductivity type epitaxial layer 2 formed on the substrate 1, and a second conductivity type body region 3 formed on the epitaxial layer 2. A U-shaped trench 4 is formed through the body region 3 to extend into the epitaxial layer 2. A gate oxide film 5 is formed on the side wall and bottom wall of the trench 4. A polysilicon gate 6 partially fills the trench so as to be surrounded by the gate oxide film 5. A silicon nitride or silicon oxide film 12 fills the portion of the trench not filled by the polysilicon gate 6. A gate electrode 9a is connected to the polysilicon gate material. A source region 7 is formed in the body region 3 to surround the trench 4. A source electrode 7a is connected to the source region 7 and a drain electrode 1a is connected to the substrate 1.

As described above, Mo was cited as disclosing all elements of the claimed invention with the exception of a gate formed of polysilicon and a metal silicide. Claim 1 has been amended to and newly added independent claim 10 recite that

the gate is formed of polycrystalline silicon and one of silicon oxide and silicon nitride. Mo fails to disclose the inclusion of an insulating material such as silicon oxide or silicon nitride in the gate of a vertical MOS transistor. Nor does the admitted prior art contain any suggestion to include an insulator in the gate of the vertical MOS transistor.

Accordingly, the claims are not rendered obvious by Mo and the admitted prior art because the combined teachings therein do not suggest the modifications that would be needed to replicate the claimed invention. In the context of obviousness rejections based upon the purported obviousness of effecting a required modification, the Federal Circuit has held that "[t]he mere fact that the prior art may be modified in [a given] manner ... does not make the modification obvious unless the prior art suggested the desirability of the modification". In re Fritch, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992). There is nothing in Mo or the admitted prior art that would have suggested altering the structure of the gate of a vertical MOS transistor to include an insulator such as an oxide or nitride of silicon.

Accordingly, applicant respectfully submits that claims 1 and 10-20 patentably distinguish over the prior art of record and that the rejection under 35 U.S.C. §103(a) should be withdrawn.

In view of the foregoing amendments and discussion, the application is now believed to be in condition for allowance. Accordingly, favorable reconsideration and allowance of the claims are most respectfully requested.

Respectfully submitted,

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE SPECIFICATION:

Paragraph beginning at line 6 of page 1 has been amended as follows:

Fig. 2 illustrates a schematic sectional view of a conventional vertical MOS transistor having a trench structure. A semiconductor substrate is prepared in which a lightly doped layer 2 of a first conductive (or conductivity) type is epitaxially grown on a heavily doped substrate 1 of the first conductive type to be a drain region. Then, a diffusion region 3 of a second conductive type referred to as a body region is formed from a surface of the semiconductor substrate by impurity implantation and high temperature thermal treatment at 1000°C or higher. Further, from the surface, a heavily doped impurity region 7 of the first conductive type to be a source region and a heavily doped body contact region 8 of the second conductive type for the purpose of fixing a potential of the body region by an ohmic contact are formed and are connected to a source electrode 7a and a body electrode 8a, respectively. Here, since a potential of the source region of the first conductive type and a potential of the body contact region of the second conductive type are usually the same, they are laid out so as to be in contact

with each other in Fig. 2. The source electrode 7a and the body electrode 8a are connected with each other through a contact hole, not shown in the figure, for electrically contacting the two regions. Then, a trench 4 is formed by etching single crystalline silicon through the source region of the first conductive type. A gate insulating film 5 and polycrystalline silicon 6 containing a high concentration of impurity to be connected to a gate electrode 9a fill the silicon trench. The heavily doped region of the first conductive type on a rear side of the semiconductor substrate is connected to a drain electrode 1a.

Paragraph beginning at line 9 of page 5 has been amended as follows:

According to another aspect of the present invention, the vertical MOS transistor is characterized in that [the] a film other than a metal silicide is formed in the trench so as to be in contact with the polycrystalline silicon gate and surrounded by the gate insulating film and the polycrystalline silicon gate, the other film being formed of [is] a silicon compound.

Paragraph beginning at line 24 of page 6 has been amended as follows:

According to another aspect of the present invention, the method of manufacturing a vertical MOS transistor is characterized in that a [the] film other than a metal silicide is formed on the polycrystalline silicon layer, such as [is] a silicon oxide film.

Paragraph beginning at line 17 of page 11 has been amended as follows:

Then, as a process specific to the present invention, first, the polycrystalline silicon 6 containing a high concentration of impurity is deposited at a thickness according to a width of the trench so as not to completely fill the trench (Fig. 5). For example, when the width of the trench is 0.8 μm, the polycrystalline silicon is deposited to a thickness of 0.2 μm. The polycrystalline silicon containing a high concentration of impurity may be formed arbitrarily such as by implanting the impurity using thermal diffusion or ion implantation after polycrystalline silicon containing no impurity is deposited or by introducing the impurity [during] while the polycrystalline silicon is being deposited.

Paragraph beginning at line 10 of page 14 has been amended as follows:

First, since the gate has a laminated structure of the conventionally used polycrystalline silicon film and the

metal silicide film, the gate resistance value can be lowered to 20% or less of that of the conventional art with only the polycrystalline silicon film. Especially, since the metal silicide reaches near the channel at a bottom portion of the trench, the inversion/depletion operation of the channel is fast, and [a] turn-on characteristics and [a] turn-off characteristics are improved. This allows a faster vertical MOS transistor, and operation at the level of MHz can be carried out effectively.

IN THE CLAIMS:

Claim 1 has been amended as follows:

1. (Amended) A vertical MOS transistor comprising:

a semiconductor substrate having [of] a first conductivity [conductive] type;

an epitaxial growth layer having the [of said] first conductivity [conductive] type formed on the [said] semiconductor substrate;

a body region having [of] a second conductivity [conductive] type formed on the [said] epitaxial growth layer;

a trench formed through the [said] body region of the [said] second conductivity [conductive] type so as to reach [an] inside of the [said] epitaxial growth layer of the [said] first conductivity [conductive] type;

a gate insulating film formed along an upper [a] surface of the [said] body region of the [said] second conductivity [conductive] type and a wall surface and a bottom surface of the [said] trench;

a polycrystalline silicon gate partially filling [formed in] the [said] trench so as to be in contact with the [said] gate insulating film and surrounded by the [said] gate insulating film;

a second [metal silicide] gate comprised of one of a silicon oxide film and a silicon nitride [as a] film filling a remaining portion of the trench not filled by the polycrystalline silicon gate [formed in said trench] so as to be in contact with the [said] polycrystalline silicon gate and surrounded by the [said] gate insulating film and the [said] polycrystalline silicon gate;

a source region of the [said] first conductivity [conductive] type formed in the upper [on said] surface of the [said] body region of the [said] second conductivity [conductive] type and around the [said] trench so as to be in contact with the [said] gate insulating film;

a gate electrode connected to the [said] polycrystalline silicon gate and the second [said metal silicide] gate;

a source electrode connected to the [said] source region; and

a drain electrode connected to the [said] semiconductor substrate.